

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

**INFORMATION DISCLOSURE  
STATEMENT**

Docket Number:  
**02885/84**

Serial No.  
**To be assigned**

Filing Date  
**Herewith**

Examiner  
**To be assigned**

Art Unit  
**To be assigned**

Invention Title  
**I/O AND MEMORY BUS SYSTEM FOR  
DFPS AS WELL AS MODULES HAVING  
TWO- OR MULTIDIMENSIONAL  
PROGRAMMABLE CELL STRUCTURES**

Inventors  
**Martin Vorbach et al.**

Commissioner for Patents  
P. O. Box 1450  
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1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicant(s) hereby bring the following reference(s) to the attention of the Examiner. The reference(s) are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b).
2. Copies of each of the cited references listed on the modified PTO form 1449 are not enclosed. Copies of each of the references were previously provided in the following parent application: U.S. Patent Application Serial No. 10/304,252.

Dated: *2 March 2004*

By: 

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449</b>	Atty. Docket No. <b>02885/84</b>	Serial No. <b>To be assigned</b>
	Applicant(s) <b>Martin Vorbach et al.</b>	
	Filing Date <b>Herewith</b>	Group Art Unit <b>To be assigned</b>

**U. S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE34363	August 31, 1993	Freeman			
	4,591,979	May 27, 1986	Iwashita			
	4,706,216	November 10, 1987	Carter			
	4,739,474	April 19, 1988	Holsztynski			
	4,761,755	August 2, 1988	Ardini, et al.			
	4,811,214	March 7, 1989	Nosenchuck et al.			
	4,852,043	July 25, 1989	Guest			
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	4,870,302	September 26, 1989	Freeman			
	4,901,268	February 13, 1990	Judd			
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	5,014,193	May 7, 1991	Garner et al.			
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	5,559,450	September 24, 1996	Ngai et al.			
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						YES	NO
	0 477 809	April 1, 1992	Europe				
	0 726 532	July 2, 1998	Europe				
	0 221 360	May 13, 1987	Europe				
	0 678 985	October 25 1995	Europe				
	0 428 327	May 22, 1991	Europe				

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	0 748 051	December 11, 1996	Europe				
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	Villasenor, John, et al., "Configurable Computing." <u>Scientific American</u> , Vol. 276, No. 6, June 1997, pp. 66-71.
	Villasenor, John, et al., "Configurable Computing Solutions for Automatic Target Recognition," <u>IEEE</u> , 1996 pp. 70-79.
	Tau, Edward, et al., "A First Generation DPGA Implementation," <u>FPD'95</u> , pp. 138-143
	Athanas, Peter, et al., "IEEE Symposium on FPGAs For Custom Computing Machines," <u>IEEE Computer Society Press</u> , April 19-21, 1995, pp. i-vii, 1-222
	"Bittner, Ray, A., Jr., "Wormhole Run-Time Reconfiguration: Conceptualization and VLSI Design of a High Performance Computing system," <u>Dissertation</u> , January 23, 1997, pp. i-xx, 1-415
	Myers, G., <u>Advances in Computer Architecture</u> , Wiley-Interscience Publication, 2nd ed., John Wiley & Sons, Inc. pp. 463-94, 1978.
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	Maxfield, C. "Logic that Mutates While-U-Wait" EDN (Bur. Ed) (USA), EDN (European Edition), 7 November 1996, Cahners Publishing, USA
	Norman, Richard S., <u>Hyperchip Business Summary, The Opportunity</u> , January 31, 2000, pages 1-3.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	